

# SG12864A ( 128 DOTS X 64 DOTS )

## FEATURES

- ◆ BUILT-IN CONTROLLER (KS0107 OR EQUIVALENT)
- ◆ +5 V POWER SUPPLY
- ◆ 1/64 DUTY CYCLE
- ◆ 8-BIT PARALLEL INTERFACE
- ◆ 4.2 V LED FORWARD VOLTAGE

## MECHANICAL DATA

ITEM	DIMENSIONS	UNIT
Module Size ( W x H x T )	93.0 x 70.0 x 8.8 ( 12.7 LED )	mm
Viewing Area ( W x H )	72.0 x 40.0	mm
Active Area ( W x H )	66.52 x 33.24	mm
Dot Size ( W x H )	0.48 x 0.48	mm
Dot Pitch ( W x H )	0.52 x 0.52	mm

## INTERFACE PIN CONNECTIONS

NO	SYMBOL	LEVEL	FUNCTION
1	Vss	0V	Power Supply Ground
2	VDD	5V	Power Supply Voltage
3	Vo	-	Contrast Adjustment Voltage
4	D/I	H/L	H : Data, L : Instruction Code
5	R/W	H/L	H : Read / L : Write
6	E	H→L	Enable Signal
7-14	DB0-DB7	H/L	Data Bus Line
15	CS1	H	Chip Select Signal For IC1
16	CS2	H	Chip Select Signal For IC2
17	/RES	L	Reset Signal
18	Vout	-	Power Supply Voltage For LCD
19	A	4.2V	LED Power (+)
20	K	0V	LED Power (-)

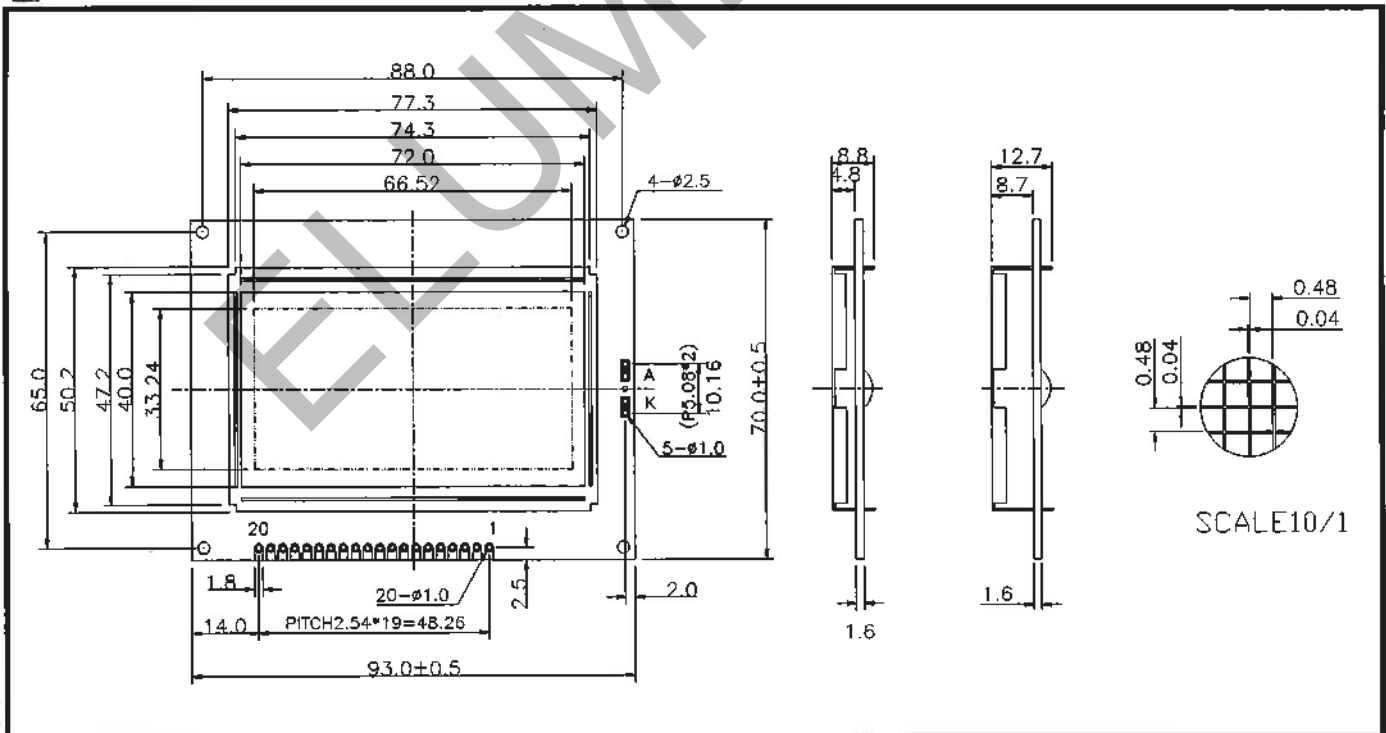
## ABSOLUTE MAXIMUM RATINGS

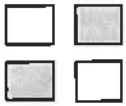
ITEM	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage For Logic	VDD-VSS	0	-	7	V
Supply Voltage For LCD Drive	VDD-Vo	0	-	14	V
Input Voltage	V <sub>I</sub>	VSS	-	VDD	V

## ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	
Supply Voltage For Logic	VDD-VSS	-	4.5	5	5.5	V	
Supply Voltage For LCD	VDD-Vo	VDD=5V Ta=25°C	7.6	8.3	9.2	V	
Supply Current	I <sub>CC</sub>	VDD=5V	-	4.5	10	mA	
Input Voltage	"HIGH" Level	V <sub>IH</sub>	-	2.2	-	VDD	V
	"LOW" Level	V <sub>IL</sub>	-	-	-	0.6	V
Output Voltage	"HIGH" Level	V <sub>OH</sub>	-	2.4	-	-	V
	"LOW" Level	V <sub>OL</sub>	-	-	-	0.4	V

## EXTERNAL DIMENSIONS





# SG12864A ( 128 DOTS X 64 DOTS )

## TIMING CHARACTERISTICS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNTT.	FIG
E Cycle Time	$t_{CYC}$	1000	-	-	ns	1,2
E High Level Width	$P_{WEH}$	450	-	-	ns	1,2
E Low Level Width	$P_{WEL}$	450	-	-	ns	1,2
E Rise Time	$t_r$	-	-	25	ns	1,2
E Fall Time	$t_f$	-	-	25	ns	1,2
Address Setup Time	$t_{AS}$	140	-	-	ns	1,2
Address Hold Time	$t_{AH}$	10	-	-	ns	1,2
Data Setup Time	$t_{DSW}$	200	-	-	ns	1
Data Delay Time	$t_{DDR}$	-	-	320	ns	2
Data Hold Time	Write	$t_{DHW}$	10	-	ns	1
Data Hold Time	Read	$t_{DHR}$	20	-	ns	2

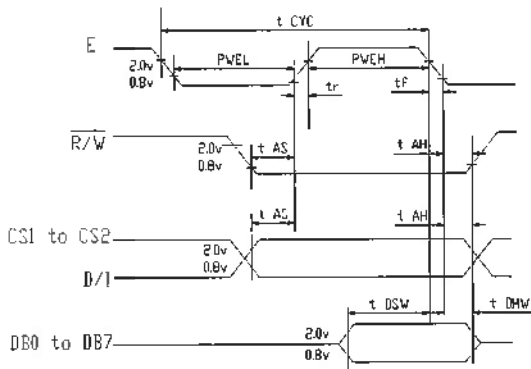


Fig1:CPU Write Timing

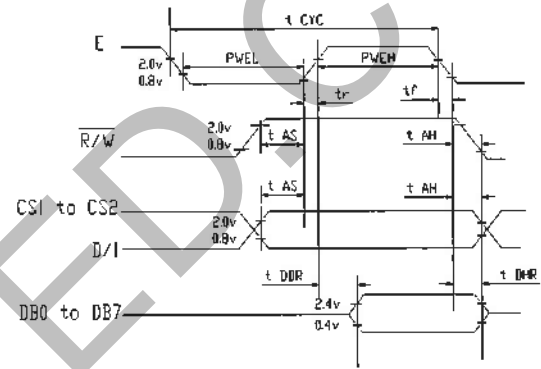


Fig2:CPU Read Timing

## BLOCK DIAGRAM

