SG12864CBW LCD MODULE

1. FEATURES

1.1 Display Type: STN

1.2 Display Mode: BLUE

1.3 Polarizer Mode: Transflective

1.4 Viewing Director: 6 O'clock

1.5 Driving Method: 1/64Duty, 1/9Bias

1.6 Backlight: LED (WHITE)

1.7 Controller & Driver: SBN0064&SBN6400

1.8 Data Transfer: 8 Bit Parallel

1..9 Dot Matrix: 128X64Dots

1.10 Dot Size: 0.48X0.48(mm)

1.11 Dot Pitch: 0.52X0.52(mm)

1.12 Operating Temperature: 0°C~+50°C

Storage Temperature: -20°C~+70°C

1.13 Conformity of RoHS

2. MECHANICAL PARAMETERS

Item	Description	Unit
LCM Outline Dimension	93.0X70.0X13.5	mm
Effective Viewing Area	70.6X38.6	mm
Weight	About 80	g

3. ELECTRICAL CHARACTERISTICS

Vdd=5V±5%,Vss=0,Ta=25℃

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	Vdd	--	4.8	5.0	5.2	V
Operating Voltage for LCD	V_{LCD}	--	--	11.6	--	V
Input Signal Voltage	Vih	--	0.7Vdd	--	Vdd	V
	Vil	--	Vss	--	0.3Vdd	V
Operating Current for LCM	Idd	Vdd=5.0V	--	2.2	4.0	mA

4. DC CHARACTERISTICS

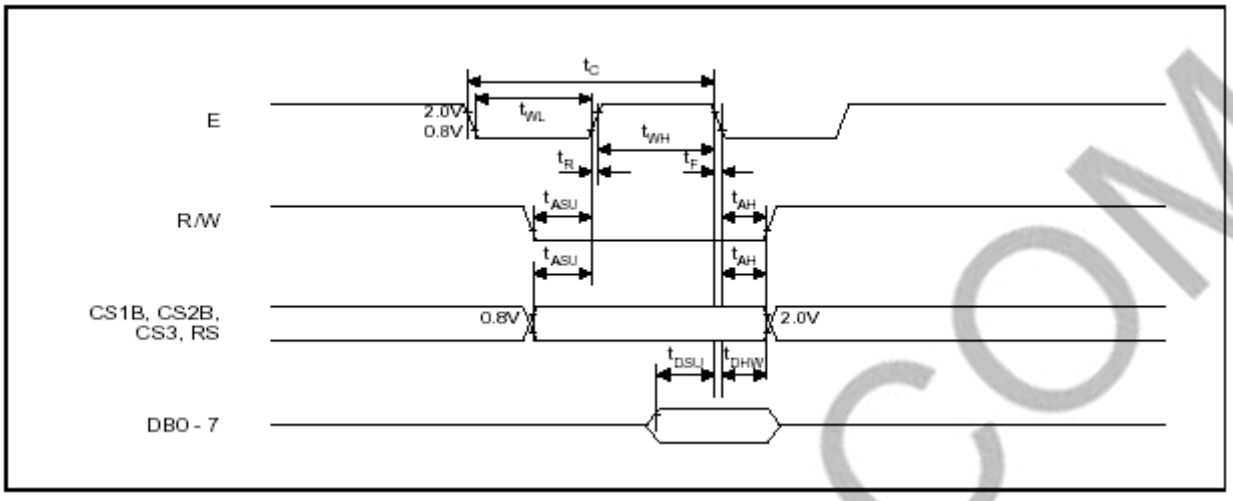
Vdd=5V±5%,Vss=0,Ta=25℃

Characteristic	Symbol	Condition	Min	Typ	Max	Unit	Note
Input high voltage	V_{IH1}	-	$0.7V_{DD}$	-	V_{DD}	V	(1)
	V_{IH2}	-	2.0	-	V_{DD}	V	(2)
Input low voltage	V_{IL1}	-	0	-	$0.3V_{DD}$	V	(1)
	V_{IL2}	-	0	-	0.8	V	(2)
Output high voltage	V_{OH}	I_{OH} = -200μA	2.4	-	-	V	(3)
Output low voltage	V_{OL}	I_{OL} = 1.6mA	-	-	0.4	V	(3)
Input leakage current	I_{LKG}	$V_{IN} = V_{SS} - V_{DD}$	-1.0	-	1.0	μA	(4)
Three-state(off) input current	I_{TSL}	$V_{IN} = V_{SS} - V_{DD}$	-5.0	-	5.0	μA	(5)
Driver input leakage current	I_{DIL}	$V_{IN} = V_{EE} - V_{DD}$	-2.0	-	2.0	μA	(6)
Operating current	I_{DD1}	During display	-	-	100	μA	(7)
	I_{DD2}	During access Access cycle = 1MHz	-	-	500	μA	(7)
On resistance	R_{ON}	V_{DD}-V_{EE} = 15V I_{LOAD} = ± 0.1mA	-	-	7.5	KΩ	(8)

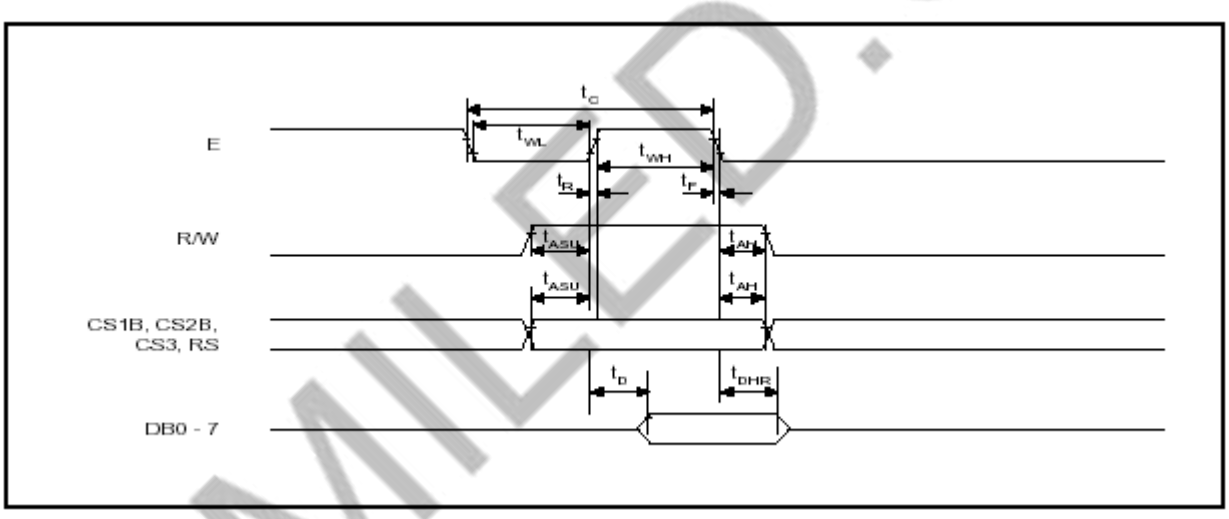
5. READ/WRITE CHARACTERISTICS

Vdd=5V±5%,Vss=0,Ta=25℃

Characteristic	Symbol	Min	Typ	Max	Unit
E cycle	t_C	1000	-	-	ns
E high level width	t_{WH}	450	-	-	ns
E low level width	t_{WL}	450	-	-	ns
E rise time	t_R	-	-	25	ns
E fall time	t_F	-	-	25	ns
Address set-up time	t_{ASU}	140	-	-	ns
Address hold time	t_{AH}	10	-	-	ns
Data set-up time	t_{DSU}	200	-	-	ns
Data delay time	t_D	-	-	320	ns
Data hold time (write)	t_{DHW}	10	-	-	ns
Data hold time (read)	t_{DHR}	20	-	-	ns

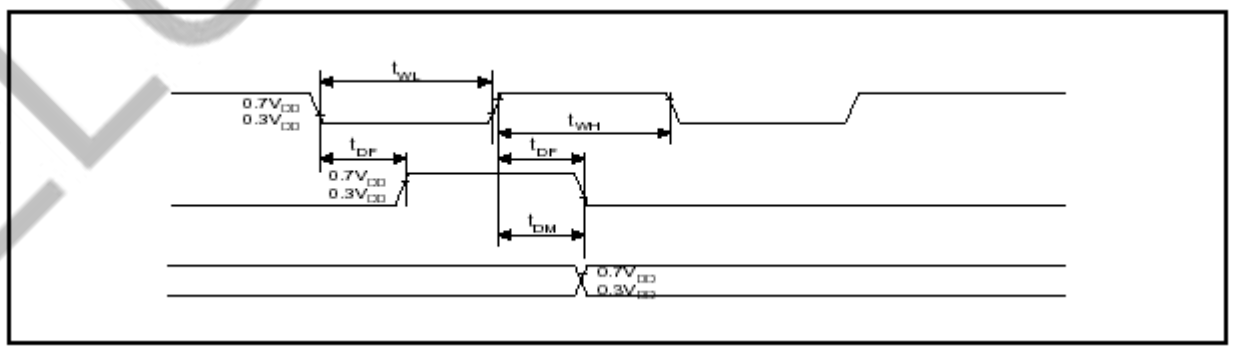


MPU Write Timing



MPU Read Timing

6. DISPLAY CONTROL TIMING



Vdd=5V±5%,Vss=0,Ta=25℃

Characteristic	Symbol	Min	Typ	Max	Unit
FRM delay time	t_{DF}	-2	-	+2	us
M delay time	t_{DM}	-2	-	+2	us
CL "low" level width	t_{WL}	35	-	-	us
CL "high" level width	t_{WH}	35	-	-	us

7.RESET TIMING

RESET

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU.

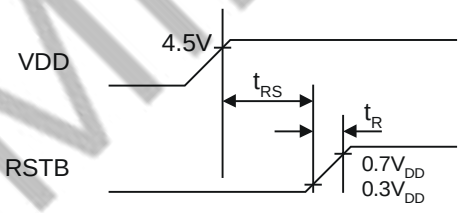
When RSTB becomes low, following procedure is occurred.

- Display off
- Display start line register become set by 0. (Z-address 0)

While RSTB is low, No instruction except status read can be accepted. Therefore, execute other instructions after making sure that DB4 = 0 (clear RSTB) and DB7 = 0 (ready) by status read instruction. The Conditions of power supply at initial power up are shown in table 1.

Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RS}	1.0	-	-	us
Rise time	t_R	-	-	200	ns



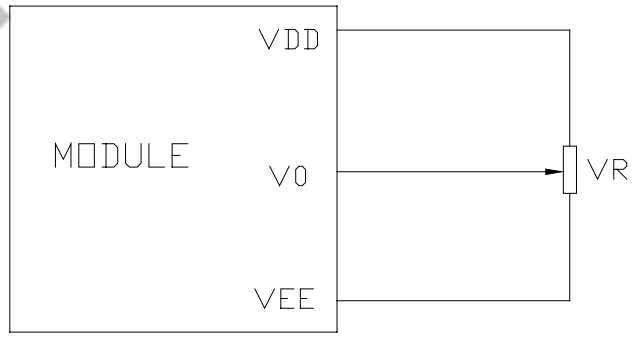
8. CONTROLS AND DISPLAY COMMAND

The display control instructions control the internal state of the S6B0108. Instruction is received from MPU to S6B0108 for the display control. The following table shows various instructions.

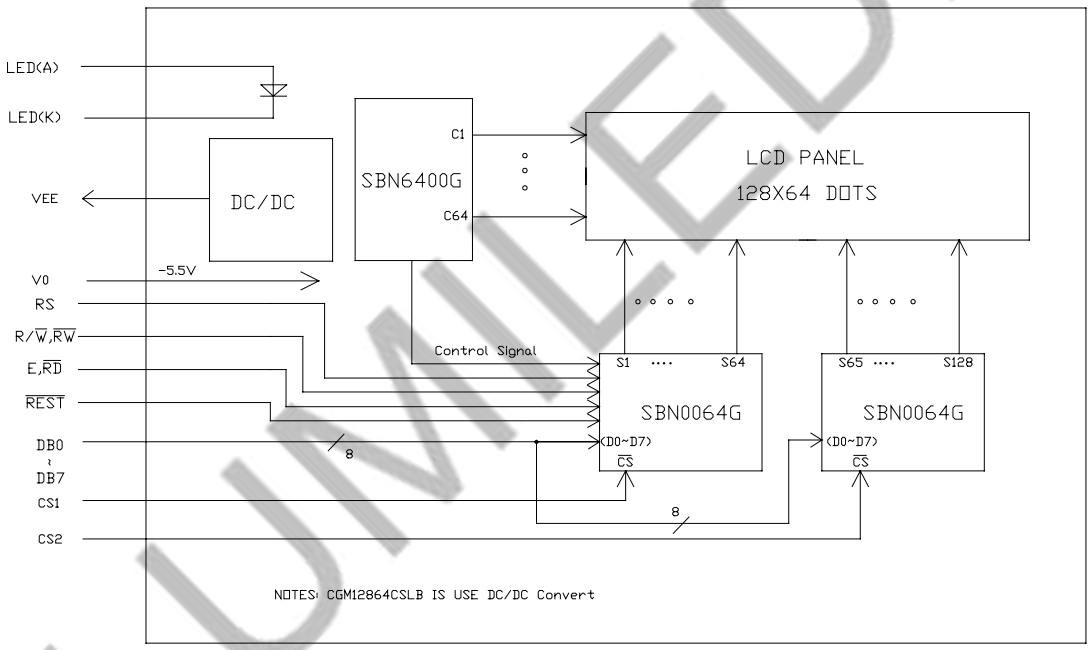
Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display on/off	L	L	L	L	H	H	H	H	H	L/H	Controls the display on or off. Internal status and display RAM data is not affected. L: OFF, H: ON
Set address (Y address)	L	L	L	H	Y address (0 - 63)						Sets the Y address in the Y address counter.
Set page (X address)	L	L	H	L	H	H	H	Page (0 - 7)			Sets the X address at the X address register.
Display start line (Z address)	L	L	H	H	Display start line (0 - 63)						Indicates the display data RAM displayed at the top of the screen.
Status read	L	H	Busy	L	On / Off	Reset	L	L	L	L	Read status. BUSY L: Ready H: In operation ON/OFF L: Display ON H: Display OFF RESET L: Normal H: Reset
Write display data	H	L	Write data								Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read display data	H	H	Read data								Reads data (DB0: 7) from display data RAM to the data bus.

9.Power Supply

It is recommended to apply a potentiometer for the contrast adjust due to the tolerance of the driving voltage and its temperature dependence.



10. SYSTEM BLOCK DIAGRAM



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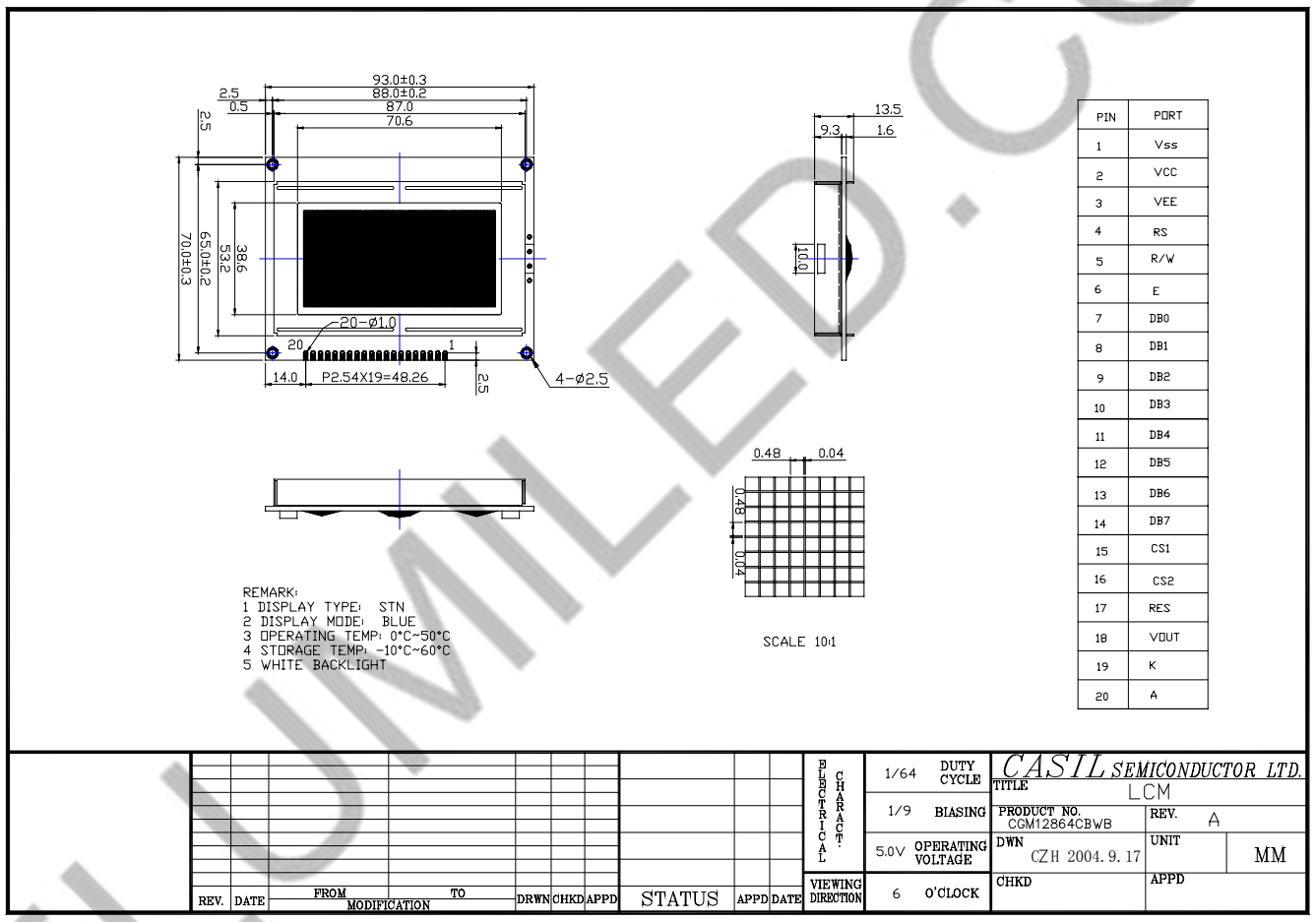
11. PIN ASSIGNMENT

Pin No.	Symbol	Level	Description
1	VSS	0V	Ground
2	VDD	+5V	Power supply for logic and LCD (+)
3	V0	--	Power supply voltage for LCD driving
4	RS	H/L	Data type selection
5	R/W	H/L	68 series R/W signal
6	E	H/L	68 series E clock
7	DB0	H/L	Data bit0
8	DB1	H/L	Data bit1
9	DB2	H/L	Data bit2
10	DB3	H/L	Data bit3
11	DB4	H/L	Data bit4
12	DB5	H/L	Data bit5
13	DB6	H/L	Data bit6
14	DB7	H/L	Data bit7
15	CS1	H	Chip select for left panel
16	CS2	H	Chip select for right panel
17	RES	L	Reset signal
18	VEE	H	Negative voltage input (Customer used)
19	LED (K)	0	LED -
20	LED (A)	4.2	LED +

SG12864AUL LCD MODULE

13、ASSEMBLY DIAGRAM



PIN	PORT
1	Vss
2	VCC
3	VEE
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	CS1
16	CS2
17	RES
18	VOUT
19	K
20	A

REV.	DATE	FROM / TO MODIFICATION	DRWN	CHKD	APPD

STATUS APPD DATE

ELECTRICAL CHARACT.

1/64	DUTY CYCLE
1/9	BIASING
5.0V	OPERATING VOLTAGE
6	O'CLOCK
VIEWING DIRECTION	

CASTL SEMICONDUCTOR LTD.

TITLE	LCM
PRODUCT NO.	CGM12864CBWB
REV.	A
DWN	CZH 2004. 9. 17
UNIT	MM
CHKD	
APPD	